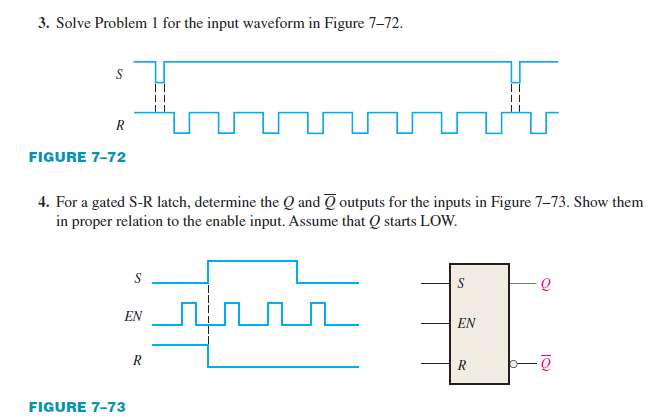
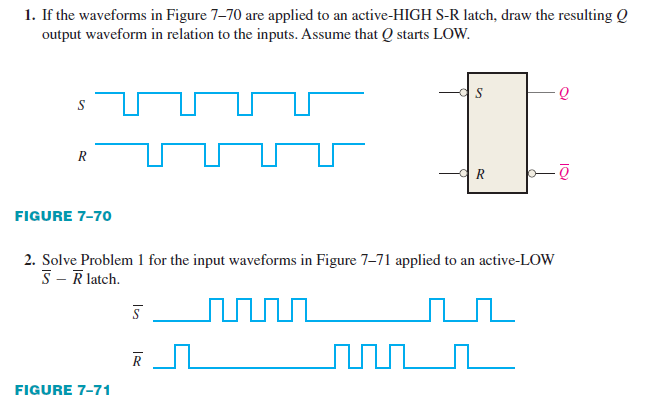
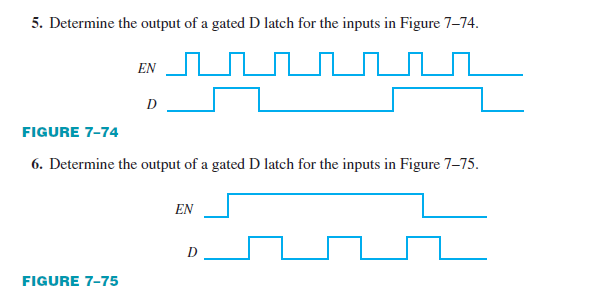
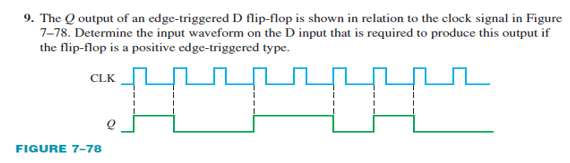
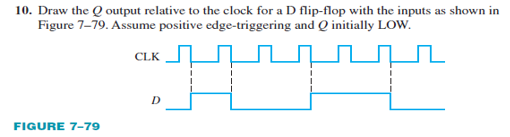
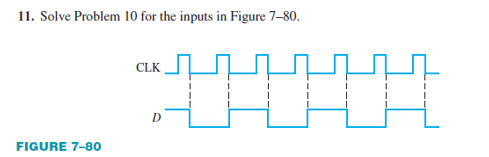
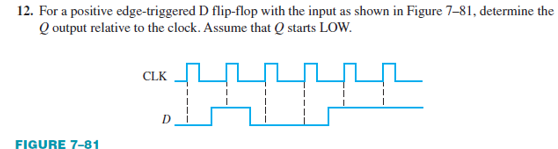
**Chapter-7 (Practice Questions )**

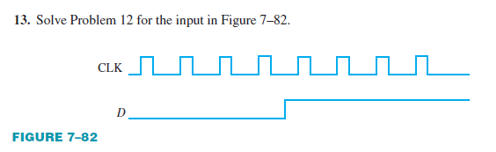


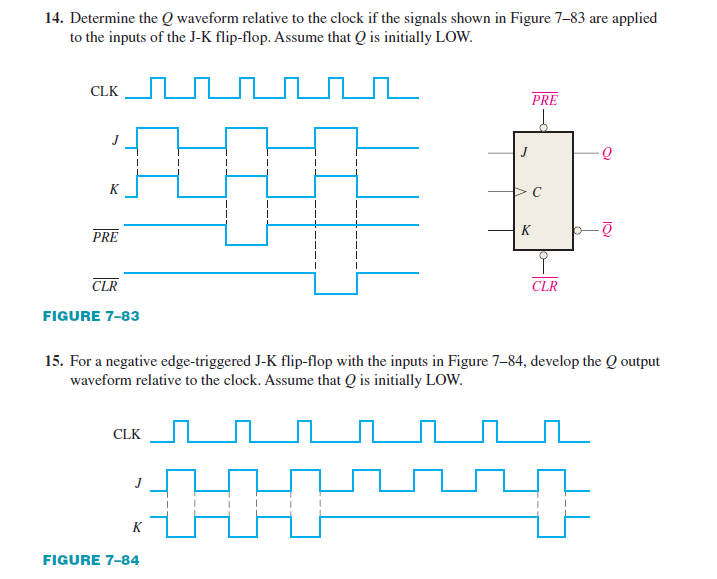


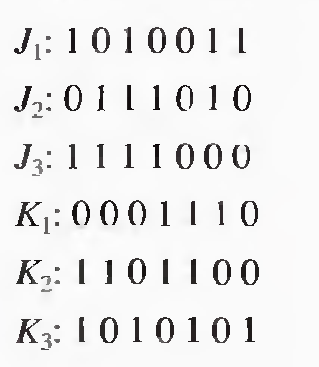
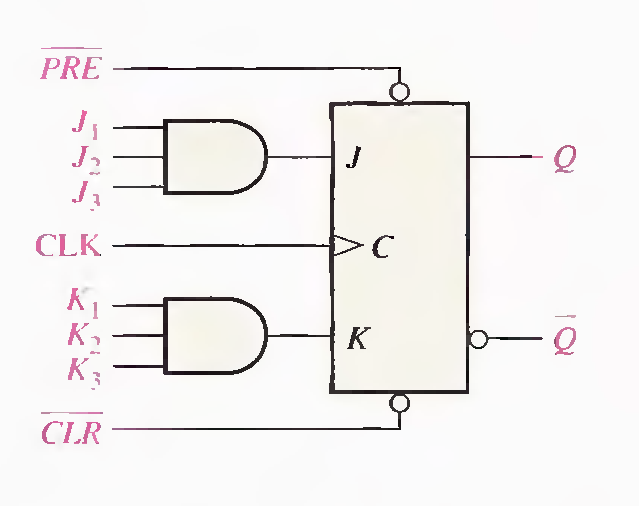




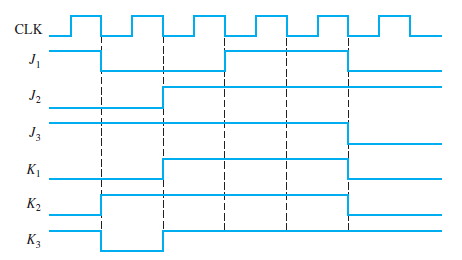




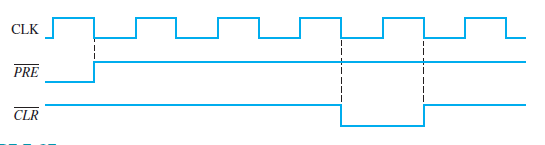
1. The following serial data are applied to the flip-flop through the AND gates as indicated in Figure. Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH. Rightmost bits are applied first.

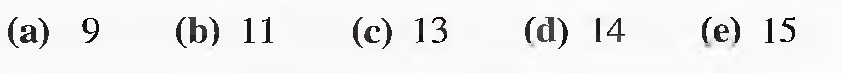
1. For the circuit in Figure -1, complete the timing diagram in Figure 2 by showing the Q output (which is initially LOW). Assume PRE and CLR remain HIGH.



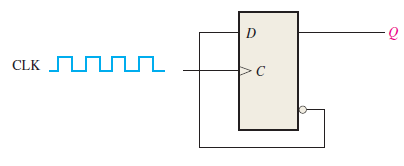
1. Solve Problem 2 with the same J and K inputs but with the PRE and CLR inputs as shown in Figure 3 in relation to the clock.



1. Show how to connect a 4-bit asynchronous counter for each of the following moduli. Also for 30kHz clock determine the frequency at the output of each counter.



1. A D flip-flop is connected as shown in Figure 7–90. Determine the Q output in relation to the clock. What specific function does this device perform?



1. For the circuit in Figure, develop a timing diagram for eight clock pulses, showing the QA and QB outputs in relation to the clock.

